4776 76215

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 10/20/02 Serial # 09/981,277 Priority Application Date 2/28/00

Your Name M. Lewis Examiner # _____

AU 2829 Phone 305-3243 Room Flax3-3800

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: **USPT** **DWPI** **EPO Abs** **JPO Abs** **IBM TDB**

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 12-20

Problem: See Page 1 lines 9-27

" " 2 " 1-27

Solution: See Abstract

& See structure illustrated in the claims

Staff Use Only

Searcher: Bode

Phone: 605 1726

EIC-EIC2800, CP4-9C18

10-22-02

10-22-02

Type of Search

Structure (#)_____

Bibliographic ✓

Litigation_____

Fulltext ✓

Patent Family_____

Other_____

Vendors

STN_____

Dialog ✓

Questel/Orbit ✓

Lexis-Nexis_____

WWW/Internet_____

Other_____

File : PLUSPAT

SS	Results	
1	0	/CT EP1225592
2	0	/CT EP1132920
3	0	/CT EP1207538

Search statement 4

```
Set     Items   Description
S1      44650   MRAM OR MAGNETIC?()RANDOM()ACCESS()MEMOR? OR (NONVOLATILE -
             OR NON(W)VOLATILE)(W)MEMORY OR NON()VOLATILE()RAM OR NVRAM OR
             MAGNET?(3N)MEMOR?
S2      80974   (MEMORY OR STORAG? OR REGISTER OR MAGNETORESIST?)(2N)CELL?
S3        267   (SDT OR SPIN()DEPEND?()TUNNEL?)(2N)JUNCTION?
S4       5188   TMR OR TUNNEL?()MAGNETORESIS?
S5        222   (BOTTOM? OR TOP OR PRIMARY? LOWER? OR UPPER? OR SECOND??? -
             PINNED OR SENSE OR FIRST? OR INITIAL? OR ORIGINAL? OR 2ND)()F-
             ERROMAGNETIC?()LAYER?
S6          0   S1 AND S2 AND S3 AND S4 AND S5
S7          2   S1 AND S2 AND S3 AND S5
S8          2   RD (unique items)
S9          6   S1 AND S2 AND S3
S10        11   S1 AND S2 AND S5
S11        15   S9 OR S10
S12        13   S11 NOT S8
S13        13   RD (unique items)
? show files
File   2:INSPEC 1969-2002/Oct W3
         (c) 2002 Institution of Electrical Engineers
File   6:NTIS 1964-2002/Oct W3
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2002/Oct W2
         (c) 2002 Engineering Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2002/Oct W3
         (c) 2002 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2002/Sep
         (c) 2002 ProQuest Info&Learning
File  65:Inside Conferences 1993-2002/Oct W3
         (c) 2002 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2002/Aug W3
         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Sep
         (c) 2002 The HW Wilson Co.
File 144:Pascal 1973-2002/Oct W3
         (c) 2002 INIST/CNRS
File 305:Analytical Abstracts 1980-2002/Oct W1
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Sep
         (c) 2002 DECHEMA
File 344:Chinese Patents Abs Aug 1985-2002/Oct
         (c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200267
         (c) 2002  Thomson Derwent
?
```

8/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07070583 **Image available**
SPIN DEPENDENT TUNNELING JUNCTION FOR **MRAM** DEVICES

PUB. NO.: 2001-298228 [JP 2001298228 A]
PUBLISHED: October 26, 2001 (20011026)
INVENTOR(s): BRUG JAMES A
TRAN LUNG T
ANTHONY THOMAS C
BHATTACHARYYA MANOJ K
NICKEL JANICE
APPLICANT(s): HEWLETT PACKARD CO (HP)
APPL. NO.: 2001-047766 [JP 20011047766]
FILED: February 23, 2001 (20010223)
PRIORITY: 00 514934 [US 2000514934], US (United States of America), February 28, 2000 (20000228)

SPIN DEPENDENT TUNNELING JUNCTION FOR **MRAM** DEVICES

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of manufacturing an **MRAM** drive comprising **spin dependent tunneling junction memory cells** .
SOLUTION: An **SDT junction** of a **memory cell** for **MRAM** devices comprises a **bottom ferromagnetic layer** having planarized peaks, an insulative tunneling barrier located on the **bottom ferromagnetic layer** , and a **top ferromagnetic layer** located on the insulative tunneling barrier.

13/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05831109 E.I. No: EIP01236534280
Title: Dynamic switching of tunnel junction MRAM cell with nanosecond field pulses
Author: Sousa, R.C.; Freitas, P.P.
Corporate Source: INESC, 1000 Lisbon, Portugal
Conference Title: 2000 International Magnetics Conference (INTERMAG 2000)
Conference Location: Toronto, Ont, Canada Conference Date: 20000409-20000412
E.I. Conference No.: 58080
Source: IEEE Transactions on Magnetics v 36 n 5 I September 2000 2000. p 2770-2772
Publication Year: 2000
CODEN: IEMGAQ ISSN: 0018-9464
Language: English

Title: Dynamic switching of tunnel junction MRAM cell with nanosecond field pulses
Abstract: **Spin dependent tunnel junctions** aimed for storage element in **MRAM** cells were switched between low and high resistance states using 20 ns current pulses on...
Identifiers: **Magnetic random access memory (MRAM) cells**

13/3,K/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07295408 **Image available**
SHORT CIRCUIT PERMISSIBLE CROSS ARRAY

PUB. NO.: 2002-163886 [JP 2002163886 A]
PUBLISHED: June 07, 2002 (20020607)
INVENTOR(s): PERNER FREDERICK A
ANTHONY THOMAS C
APPLICANT(s): HEWLETT PACKARD CO (HP)
APPL. NO.: 2001-274444 [JP 20011274444]
FILED: September 11, 2001 (20010911)
PRIORITY: 00 663752 [US 2000663752], US (United States of America), September 15, 2000 (20000915)

ABSTRACT
PROBLEM TO BE SOLVED: To overcome problems relating to the short-circuited **SDT junction** device in the resistive **cell** cross **memory** array.

SOLUTION: The data storage device 8 includes resistive cross array 10. Each **memory cell** 12 includes **memory** element and resistive element 56 connected to the memory element 50. The resistive element 56...
... that flows through short-circuited memory elements. The data storage device 8 can be a **magnetic random access memory (MRAM)**.

13/3,K/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06975761 **Image available**
MRAM HAVING INTEGRATED SEMICONDUCTOR DEVICE

PUB. NO.: 2001-203332 [JP 2001203332 A]
PUBLISHED: July 27, 2001 (20010727)
INVENTOR(s): TEHRANI SAIED
SCHI JING
APPLICANT(s): MOTOROLA INC

APPL. NO.: 2000-361340 [JP 2000361340]
FILED: November 28, 2000 (20001128)
PRIORITY: 99 460056 [US 99460056], US (United States of America), December 13, 1999 (19991213)

MRAM HAVING INTEGRATED SEMICONDUCTOR DEVICE

ABSTRACT

... memory and increase a density of a chip by integrating an active device in the **memory** element.

SOLUTION: A magnetic **memory cell** 10 has a semiconductor layer 12 which is formed between a 1st ferromagnetic layer 11 and a **2nd ferromagnetic layer** 13 by a p-n junction or a Schottky junction. An antiferromagnetic layer 34 is provided between the **2nd ferromagnetic layer** 13 and a digit line 35 in order to fix a magnetization vector in the **2nd ferromagnetic layer** . Gate contacts 37 are separated from the semiconductor layer 12 in order to control the...

13/3,K/4 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06179209 **Image available**
NONVOLATILE RANDOM ACCESS MEMORY

PUB. NO.: 11-120758 [JP 11120758 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): ERIC MAIKEN
APPLICANT(s): SONY CORP
APPL. NO.: 09-277687 [JP 97277687]
FILED: October 09, 1997 (19971009)

ABSTRACT

...shortening a read time and reducing power consumption.

SOLUTION: This memory is constituted by allowing **memory cells** whose **memory** states are able to be changed over by the injecting of spinningly polarized electrons to be arranged. Concretely, the **memory cell** is constituted by allowing, for example, a **first ferromagnetic layer** and a second ferromagnetic layer to be laminated with a normal magnetic layer 13 and the direction of the magnetization of the **first ferromagnetic layer** is fixed and a memory state is changed over by the direction of the magnetization...
... propagation theory of a spinningly polarized electron flow as a new technology storing information in **magnetic memory cells** and is assemblable with the array of mesoscopic multilayer metallic devices. Then, the memory state...

... film switching layer. These states are switchable by injecting a shinningly plarized electron flow in **memory cells** .

13/3,K/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014700846 **Image available**
WPI Acc No: 2002-521550/200256
XRPX Acc No: N02-412691
Magnetic random access memory **has** magnetic spin dependent tunneling junctions **with barriers having underoxidized or undernitrided base material**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: NICKEL J H
Number of Countries: 029 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1207538	A1	20020522	EP 2001309220	A	20011031	200256	B
US 6429497	B1	20020806	US 2000715476	A	20001118	200259	
CN 1354519	A	20020619	CN 2001140855	A	20010918	200263	
JP 2002208683	A	20020726	JP 2001345805	A	20011112	200264	

Priority Applications (No Type Date): US 2000715476 A 20001118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1207538	A1	E	10	H01F-010/32	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 6429497	B1			H01L-029/76	
CN 1354519	A			H01L-027/02	
JP 2002208683	A		6	H01L-027/105	

Magnetic random access memory **has** magnetic spin dependent tunneling junctions **with barriers having underoxidized or undernitrided base material**

Abstract (Basic):

... An array (10) of **memory cells** (12) includes **magnetic spin dependent tunneling** (**SDT**) **junctions** with tunnel barriers having underoxidized or undernitrided base material. The density of the base material...

... **MRAM** with **spin dependent tunneling** (**SDT**) **junctions** . The **SDT junctions** are used in high voltage applications such as flat emitter devices, high current devices...

...discharge, handling errors and circuit anomalies. The higher breakdown voltage improves the robustness of the **SDT junctions** , improves manufacturing yield and reduces the cost of correcting bit errors...

...The figure illustrates a **MRAM** device including **SDT junctions** having partially processed base material in the tunnel junctions...

... **Memory cell** array (10...

... **Memory cells** (12

13/3,K/6 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014549663 **Image available**
WPI Acc No: 2002-370366/200240
XRAM Acc No: C02-104859
XRPX Acc No: N02-289275

Magnetic tunnel junction device for external magnetic field-sensing application, e.g. magnetic read sensor, includes tunnel barrier layer between ferromagnetic layers

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CHILDRESS J R; GURNEY B A; SCHWICKERT M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6347049	B1	20020212	US 2001916077	A	20010725	200240	B

Priority Applications (No Type Date): US 2001916077 A 20010725
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6347049	B1		10	G11C-011/15	

Abstract (Basic):

... has a first barrier layer of insulating material formed on and in contact with the **first ferromagnetic layer** and a second barrier layer of insulating material located between the first barrier

layer and...
Technology Focus:
... Preferred Components: The device is a magnetoresistive read head or **magnetic memory cell** . The **magnetic** moments of the ferromagnetic layers are oriented perpendicular to one another in the absence of...

13/3,K/7 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014175909 **Image available**
WPI Acc No: 2001-660137/200176
XRPX Acc No: N01-492324
Magnetic memory cell **for hard disc drive, has closed magnetic circuit layer arranged on surface of** upper ferromagnetic layer
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001273759	A	20011005	JP 200087389	A	20000327	200176	B

Priority Applications (No Type Date): JP 200087389 A 20000327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001273759	A		11	G11C-011/15	

Magnetic memory cell **for hard disc drive, has closed magnetic circuit layer arranged on surface of** upper ferromagnetic layer

Abstract (Basic):
... 22,24). A closed magnetic circuit layer (25) is arranged on the surface of the **upper ferromagnetic layer** (24).
... An INDEPENDENT CLAIM is also included for **magnetic memory** .
...

...Used in **magnetic memory** (claimed) and hard disc drive (HDD...

...Since closed magnetic layer is provided, width of the **magnetic memory** is reduced, and the influence of counter magnetic field is avoided. Hence magnetization is stabilized and outstanding **magnetic memory cell** is obtained...

...The figure shows a cross-sectional view of **magnetic memory cell** .

13/3,K/8 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014051211 **Image available**
WPI Acc No: 2001-535424/200159
Related WPI Acc No: 2001-519842; 2001-595082
XRPX Acc No: N01-397551
Read circuit has first direct injection preamplifier coupled to first input node of differential amplifier and has second direct injection preamplifier coupled to second input node of differential amplifier
Patent Assignee: PERNER F A (PERN-I)
Inventor: PERNER F A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010012228	A1	20010809	US 2000498587	A	20000204	200159	B
			US 2000745103	A	20001219		

Priority Applications (No Type Date): US 2000745103 A 20001219; US 2000498587 A 20000204

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20010012228 A1   8 G11C-007/02   CIP of application US 2000498587
                                      CIP of patent US 6185143

Abstract (Basic):
... An information storage device includes a resistive crosspoint **memory cell** array. A first direct injection preamplifier (32) is coupled to the first input node (S1...
... Improves detection of resistance states of **spin dependent tunneling** (**SDT**) **junctions** in **magnetic random access memory** (**MRAM**) devices. Improves detection of resistance states of **memory cell** components in resistive cross point **memory cell** arrays...

13/3,K/9 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013655286 **Image available**
WPI Acc No: 2001-139498/200115
XRAM Acc No: C01-041291
XRPX Acc No: N01-101635
Production of a magnetic tunnel contact comprises depositing a metal layer on a first ferromagnetic layer and oxidizing with the support of UV light to produce an insulating layer
Patent Assignee: FORSCHUNGSZENTRUM JUELICH GMBH (KERJ)
Inventor: KOHLSTEDT H; ROTTLAENDER P
Number of Countries: 022 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19938215	A1	20010222	DE 1038215	A	19990812	200115	B
WO 200113387	A1	20010222	WO 2000EP7012	A	20000721	200115	
EP 1203382	A1	20020508	EP 2000949391	A	20000721	200238	
			WO 2000EP7012	A	20000721		

Priority Applications (No Type Date): DE 1038215 A 19990812
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
DE 19938215   A1   5 H01L-029/82
WO 200113387 A1 G   H01F-041/30
  Designated States (National): JP KR US
  Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
EP 1203382   A1 G   H01F-041/30   Based on patent WO 200113387
  Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Production of a magnetic tunnel contact comprises depositing a metal layer on a first ferromagnetic layer and oxidizing with the support of UV light to produce an insulating layer

Abstract (Basic):
... Production of a magnetic tunnel contact comprises depositing a metal layer on a **first ferromagnetic layer** (1) and oxidizing with the support of UV light to produce an insulating layer (3...
... Used in the production of **memory cells** and **magnetic** field sensors (claimed), especially DRAMs, FRAMs and MRAMs...

... **first ferromagnetic layer** (1

13/3,K/10 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013627254 **Image available**
WPI Acc No: 2001-111462/200112
XRAM Acc No: C01-032954
XRPX Acc No: N01-081837

Magnetic tunnel junction sensor used as a magnetic field sensor in magnetic disk drives, has antiferromagnetic layer, pinned layer, free layer of ferromagnetic material, and tunnel barrier layer

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: GILL H H S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6127045	A	20001003	US 9878898	A	19980513	200112	B

Priority Applications (No Type Date): US 9878898 A 19980513
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6127045	A		12	H01F-001/00	

Abstract (Basic):
... sensor is used as a magnetic field sensor in magnetic disk drives or as a **memory cell** in a **magnetic** random access array (**MRAM**).

Technology Focus:
... The **first ferromagnetic layer** and first sub-layer are each made of nickel-iron (Ni40-Fe60) or cobalt-iron...

13/3,K/11 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013157928 **Image available**
WPI Acc No: 2000-329801/200029
XRPX Acc No: N00-282909
Magnetic tunnel junction magnetoresistive sensor for magnetic disk drive, has antiparallel pinned layer comprising two ferromagnetic layers with antiparallel coupling layers in between

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: GILL H S
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1245952	A	20000301	CN 99110657	A	19990720	200029	B
US 6052263	A	20000418	US 98138120	A	19980821	200033	
JP 2000067418	A	20000303	JP 99227028	A	19990811	200029	
KR 2000016943	A	20000325	KR 9928648	A	19990715	200104	
SG 77708	A1	20010116	SG 993850	A	19990807	200109	

Priority Applications (No Type Date): US 98138120 A 19980821
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1245952	A			G11B-005/127	
US 6052263	A		6	G11B-005/39	
JP 2000067418	A		11	G11B-005/39	
KR 2000016943	A			G11B-005/39	
SG 77708	A1			G11B-005/187	

Abstract (Basic):
... The AP pinned layer has a **first ferromagnetic layer** made of a material having a saturation magnetization greater than the magnetization of permalloy and...

...sublayer of soft ferromagnetic material having a near zero magnetorestriction coefficient is separated from the **first ferromagnetic layer** of the pinned layer by a tunnel barrier layer made of insulating material...

...The MTJ sensor is used in magnetic disk drive or as a **memory cell** in a **magnetic random access memory** (**MRAM**).

13/3,K/12 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012689505 **Image available**
WPI Acc No: 1999-495614/199942
XRAM Acc No: C99-145457
XRPX Acc No: N99-369300
Forming tunnel junction useful in magnetic flux heads for recording heads
Patent Assignee: HEWLETT-PACKARD CO (HEWP); ANTHONY T C (ANTH-I)
Inventor: ANTHONY T C
Number of Countries: 028 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 929110	A1	19990714	EP 99300005	A	19990104	199942 B
CN 1222771	A	19990714	CN 98122589	A	19981125	199946
JP 2000012365	A	20000114	JP 98349432	A	19981209	200014
US 6169303	B1	20010102	US 983320	A	19980106	200103
US 20020114972	A1	20020822	US 983320	A	19980106	200258
			US 2000672794	A	20000211	

Priority Applications (No Type Date): US 983320 A 19980106; US 2000672794 A 20000211
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 929110	A1	E	7	H01L-043/08	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
CN 1222771	A			H01L-043/08	
JP 2000012365	A		6	H01F-041/14	
US 6169303	B1			H01L-029/76	
US 20020114972	A1			H01L-029/76	Div ex application US 983320 Div ex patent US 6169303

Abstract (Basic):
... Forming a tunnel junction comprises forming a **first ferromagnetic layer** (12) with an upper surface having domed areas and intervening low areas and forming an...
... b) a tunnel junction comprising a thin interface layer, between a **first ferromagnetic layer** (12) and an insulating layer (14), selected to enhance magnetic polarization properties of the first...

...heads used e.g. in magnetic tape or disc recording heads. Also useful as magnetic **storage** cells in **magnetic memory** .

13/3,K/13 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011424033 **Image available**
WPI Acc No: 1997-401940/199737
Related WPI Acc No: 1996-476404; 1997-280364; 1997-393034; 2000-430059; 2001-201430; 2001-662088; 2002-265995; 2002-360247; 2002-517496
XRPX Acc No: N97-334326
Magnetic spin injected field effect transistor for e.g. non - volatile memory **store - has two ferromagnetic layers of differing coercivities electrically coupled to high conductance regions with channel connecting high conductance regions**
Patent Assignee: JOHNSON M B (JOHN-I)
Inventor: JOHNSON M B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5654566	A	19970805	US 95425884	A	19950421	199737 B
			US 95493815	A	19950622	
			US 96643804	A	19960506	

Priority Applications (No Type Date): US 96643804 A 19960506; US 95425884 A 19950421; US 95493815 A 19950622

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5654566	A		22	H01L-029/82	CIP of application US 95425884 CIP of application US 95493815 CIP of patent US 5565695

Magnetic spin injected field effect transistor for e.g. non - volatile memory **store...**

...Abstract (Basic): The magnetic spin injected transistor device (100) includes two separated high conductance regions. A **first ferromagnetic layer** (110) has a first coercivity and is electrically coupled to the first high conductance region...

...The **first ferromagnetic layer** can be set to a first magnetization orientation, the second ferromagnetic layer can be set...

...USE/ADVANTAGE - Also for digital electronics. Decreases size of device. Requires only single element in **memory cell** . Eliminates susceptibility to background radiation...

?

```
Set      Items   Description
S1          76   AU=(NICKEL, J? OR NICKEL J?)
S2       34987   MRAM OR MAGNETIC?()RANDOM()ACCESS()MEMOR? OR (NONVOLATILE -
             OR NON(W)VOLATILE)(W)MEMORY OR NON()VOLATILE()RAM OR NVRAM
S3          11   S1 AND S2
S4          23   (SDT OR SPIN()DEPEND?()TUNNEL?)(2N)JUNCTION?
S5           8   S3 AND S4
S6           8   IDPAT (sorted in duplicate/non-duplicate order)
S7           4   IDPAT (primary/non-duplicate records only)
? show files
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2002/Oct W02
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021017,UT=20021003
         (c) 2002 WIPO/Univentio
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200267
         (c) 2002  Thomson Derwent
?
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7/5,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014700846 **Image available**
WPI Acc No: 2002-521550/200256
XRPX Acc No: N02-412691
Magnetic random access memory **has magnetic** spin dependent tunneling junctions **with barriers having underoxidized or undernitrided base material**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: **NICKEL J H**
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1207538	A1	20020522	EP 2001309220	A	20011031	200256	B
US 6429497	B1	20020806	US 2000715476	A	20001118	200259	
CN 1354519	A	20020619	CN 2001140855	A	20010918	200263	
JP 2002208683	A	20020726	JP 2001345805	A	20011112	200264	

Priority Applications (No Type Date): US 2000715476 A 20001118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1207538	A1	E	10	H01F-010/32	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 6429497	B1			H01L-029/76	
CN 1354519	A			H01L-027/02	
JP 2002208683	A		6	H01L-027/105	

Abstract (Basic): EP 1207538 A1
NOVELTY - An array (10) of memory cells (12) includes magnetic **spin dependent tunneling** (**SDT**) **junctions** with tunnel barriers having underoxidized or undernitrided base material. The density of the base material at one surface of the barrier, is lower than that in other surface.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) Method of fabricating a magnetic tunnel junction; and
(2) Magnetic tunnel junction.
USE - **MRAM** with **spin dependent tunneling** (**SDT**) **junctions** . The **SDT junctions** are used in high voltage applications such as flat emitter devices, high current devices.
ADVANTAGE - The underoxidized or undernitrided material increases the breakdown voltage and reduces the chances of damage due to electrostatic discharge, handling errors and circuit anomalies. The higher breakdown voltage improves the robustness of the **SDT junctions** , improves manufacturing yield and reduces the cost of correcting bit errors.
DESCRIPTION OF DRAWING(S) - The figure illustrates a **MRAM** device including **SDT junctions** having partially processed base material in the tunnel junctions.
Memory cell array (10)
Memory cells (12)
pp; 10 DwgNo 3/4
Title Terms: MAGNETIC; RANDOM; ACCESS; MEMORY; MAGNETIC; SPIN; DEPEND; JUNCTION; BARRIER; BASE; MATERIAL
Derwent Class: U14; V02
International Patent Class (Main): H01F-010/32; H01L-027/02; H01L-027/105; H01L-029/76
International Patent Class (Additional): G11C-011/02; G11C-011/14; G11C-011/15; G11C-011/16; H01F-041/30; H01L-027/10; H01L-043/00; H01L-043/08
File Segment: EPI

Magnetic random access memory **has magnetic** spin dependent tunneling junctions **with barriers having underoxidized or undernitrided base material**
Inventor: **NICKEL J H**

Abstract (Basic):

... An array (10) of memory cells (12) includes magnetic **spin dependent tunneling (SDT) junctions** with tunnel barriers having underoxidized or undernitrided base material. The density of the base material...

... **MRAM** with **spin dependent tunneling (SDT) junctions** . The **SDT junctions** are used in high voltage applications such as flat emitter devices, high current devices...

...discharge, handling errors and circuit anomalies. The higher breakdown voltage improves the robustness of the **SDT junctions** , improves manufacturing yield and reduces the cost of correcting bit errors...

...The figure illustrates a **MRAM** device including **SDT junctions** having partially processed base material in the tunnel junctio

Magnetic Random Acc ss Memory with improv d br akdown voltage

Patent Number: EP1207538
Publication date: 2002-05-22

Inventor(s): NICKEL JANICE H (US)
Applicant(s): HEWLETT PACKARD CO (US)

Requested Patent: ☐ EP1207538
Application EP20010309220 20011031
Priority Number(s): US20000715476 20001118
IPC Classification: H01F10/32; H01F41/30; G11C11/16
EC Classification: H01F41/30D, G11C11/15, G11C11/16,
Equivalents: CN1354519, ☐ JP2002208683, ☐ US6429497
Cited patent(s): US5940319; US5986858

Abstract

A magnetic tunnel junction (30) includes a tunnel barrier (40) having partially processed (e.g. underoxidized), base material. Such magnetic tunnel junctions (30) may be used in Magnetic Random Access Memory ("MRAM") devices (8). The partially processed base material substantially increases breakdown voltage of the junction. 

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 30 9220

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 5 940 319 A (KERSZYKOWSKI GLORIA ET AL) 17 August 1999 (1999-08-17)	1,2,4,6	H01F10/32 H01F41/30
A	* claims 9,11 * * column 3, line 13 - line 14 * * column 4, line 20 - line 22 * * figure 9 *	7-9	G11C11/16
Y	US 5 986 858 A (KOBAYASHI KAZUO ET AL) 16 November 1999 (1999-11-16)	1,2,4,6	
X	* claims 1-5 * * column 1, line 1 * * column 6, line 11 - line 27 * * column 13, line 32 - line 35 * * figure 13 *	7-9	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01F
G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 February 2002	Stichauer, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 9220

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

15-02-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5940319 A	17-08-1999	US 6174737 B1	16-01-2001
US 5986858 A	16-11-1999	JP 2871670 B2	17-03-1999
		JP 11168249 A	22-06-1999
		DE 19813250 A1	17-12-1998
		KR 266353 B1	15-09-2000
		US 6165287 A	26-12-2000
		CN 1213866 A	14-04-1999
		DE 19818547 A1	15-04-1999
		US 6110751 A	29-08-2000

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

7/5,K/3 **(Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

014286990 **Image available**
WPI Acc No: 2002-107691/200215
XRPX Acc No: N02-080169
Memory cell spin dependent tunneling junction for MRAM has upper ferromagnetic layer provided on top of insulating tunnel barrier which is provided on top of lower ferromagnetic layer
Patent Assignee: HEWLETT-PACKARD CO (HEWP); NICKEL J (NICK-I)
Inventor: ANTHONY T C; BHATTACHARYYA M K; BRUG J A; **NICKEL J** ; TRAN L T
Number of Countries: 028 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1132920	A2	20010912	EP 2001301769	A	20010227	200215 B
JP 2001298228	A	20011026	JP 200147766	A	20010223	200215
US 20020047145	A1	20020425	US 2000514934	A	20000228	200233
			US 2001981277	A	20011017	

Priority Applications (No Type Date): US 2000514934 A 20000228; US 2001981277 A 20011017
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1132920	A2	E	10	G11C-011/16	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

JP 2001298228	A	9	H01L-043/08	
US 20020047145	A1		H01L-029/94	Div ex application US 2000514934

Abstract (Basic): EP 1132920 A2
NOVELTY - An insulating tunnel barrier (40) is provided on top of a lower ferromagnetic layer (46) having flattened peaks. An upper ferromagnetic layer (48) is provided on top of the insulating tunnel barrier.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a **MRAM** device for data storage;
(b) and a method for manufacturing **MRAM** .
USE - For **magnetic random access memory** (**MRAM**) for data storage.
ADVANTAGE - Reduction of storage capacity of **MRAM** device is prevented since unusable **SDT junctions** are eliminated. Increase in manufacturing cost is also prevented. Improves uniformity of resistance across **MRAM** device. Usable number of **SDT junctions** in **MRAM** device is also increased.
DESCRIPTION OF DRAWING(S) - The figure shows the diagram of an **MRAM** memory cell including **spin dependent tunneling** (**SDT**) **junction** .
Insulating tunnel barrier (40)
Lower ferromagnetic layer (46)
Upper ferromagnetic layer (48)
pp; 10 DwgNo 2/7
Title Terms: MEMORY; CELL; SPIN; DEPEND; JUNCTION; UPPER; FERROMAGNETIC; LAYER; TOP; INSULATE; TUNNEL; BARRIER; TOP; LOWER; FERROMAGNETIC; LAYER
Derwent Class: U14
International Patent Class (Main): G11C-011/16; H01L-029/94; H01L-043/08
International Patent Class (Additional): G11C-011/14; G11C-011/15; H01F-010/14; H01F-010/32; H01L-027/105; H01L-043/12
File Segment: EPI

Memory cell spin dependent tunneling junction for MRAM has upper ferromagnetic layer provided on top of insulating tunnel barrier which is provided on...
...Inventor: **NICKEL J**

Abstract (Basic):
... a) a **MRAM** device for data storage...

...b) and a method for manufacturing **MRAM** .

...

...For **magnetic random access memory** (**MRAM**) for data storage...

...Reduction of storage capacity of **MRAM** device is prevented since unusable **SDT junctions** are eliminated. Increase in manufacturing cost is also prevented. Improves uniformity of resistance across **MRAM** device. Usable number of **SDT junctions** in **MRAM** device is also increased...

...The figure shows the diagram of an **MRAM** memory cell including **spin dependent tunneling** (**SDT**) **junction** .

MRAM devic

Patent Number: EP1132920

Publication date: 2001-09-12

Inventor(s): BHATTACHARYYA MANOJ K (US); NICKEL JANICE (US); TRAN LUNG T (US); BRUG JAMES A (US); ANTHONY THOMAS C (US)

Applicant(s): HEWLETT PACKARD CO (US)

Requested Patent: ☐ EP1132920, A3

Application Number: EP20010301769 20010227

Priority Number (s): US20000514934 20000228

IPC Classification: G11C11/16

EC Classification: G11C11/16

Equivalents: ☐ JP2001298228

Cited patent(s): EP0929110; US6016241; US5764567

Abstract

A spin dependent tunneling ("SDT") junction (30) of a memory cell for a Magnetic Random Access Memory ("MRAM") device (8) includes a pinned ferromagnetic layer (38), followed by an insulating tunnel barrier (40) and a sense ferromagnetic layer (46). During fabrication of the MRAM device (8), after formation of the pinned layer (38) but before formation of the insulating tunnel barrier (40), an exposed surface of the pinned layer (38) is flattened. The exposed surface of the pinned layer (38) may be flattened by an ion etching process (110).

7/5,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01438986
Information storage device
Datenspeicheranordnung
Dispositif de memoire de donnees
PATENT ASSIGNEE:
Hewlett-Packard Company, (206037), 3000 Hanover Street, Palo Alto, CA 94304, (US), (Applicant designated States: all)
INVENTOR:
Nickel, Janice H. , 1772 Kimberly Drive, Sunnyvale, California 94087, (US)
Tran, Lung T., 5085 Woodbrae Ct., Saratoga, California 95070, (US
LEGAL REPRESENTATIVE:
Jehan, Robert et al (72663), Williams, Powell & Associates, 4 St Paul's Churchyard, London EC4M 8AY, (GB)
PATENT (CC, No, Kind, Date): EP 1225592 A2 020724 (Basic)
APPLICATION (CC, No, Date): EP 2001310276 011207;
PRIORITY (CC, No, Date): US 758757 010111
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G11C-011/16

ABSTRACT EP 1225592 A2
A magnetic memory element (10) is written to by heating the memory element (10) and applying at least one magnetic field (Hx, Hy) to the memory element (10). More reliable storage is afforded thereby.
ABSTRACT WORD COUNT: 35
NOTE:
Figure number on first page: 3

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020724 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200230	231
SPEC A	(English)	200230	2803
Total word count - document A			3034
Total word count - document B			0
Total word count - documents A + B			3034

INVENTOR:
Nickel, Janice H ...

...SPECIFICATION A2
The present invention relates to information storage devices, such as **Magnetic Random Access Memory** (" **MRAM** ") devices.
Consider the example of an **MRAM** device including a resistive cross-point array of **spin dependent tunnelling** (**SDT**) **junctions** , word lines extending along rows of the **SDT junctions** , and bit lines extending along columns of the **SDT junctions** . Each **SDT junction** is located at a cross-point of a word line and a bit line. The magnetisation of each **SDT junction** assumes one of two stable orientations at any given time. These two stable orientations, parallel ...

...values of '0' and '1'. The magnetisation orientation, in turn, affects the resistance of the **SDT junction** . Resistance of the **SDT junction** is a first value (R) if the magnetisation orientation is parallel and a second value (R+(DELTA)R) if the magnetisation orientation is anti-parallel. The magnetisation orientation of the **SDT junction** and, therefore, its logic value may be read by sensing its resistance state.
A write operation on a selected **SDT junction** is performed by supplying write currents to the word and bit lines crossing the selected **SDT junction** . The currents create two external magnetic fields that,

when combined, switch the magnetisation orientation of the selected **SDT junction** from parallel to anti-parallel or vice versa.

Too small a write current might not cause the selected **SDT junction** to change its magnetisation orientation. In theory, both external fields combined should be sufficient to flip the magnetisation orientation of the selected **SDT junction** . In practice, however, the combined magnetic fields do not always flip the magnetisation orientation. If the magnetisation orientation of the selected **SDT junction** is not flipped, a write error is made and an increased burden on error code correction can result.

SDT junctions that see only one magnetic field (that is, **SDT junctions** along either a selected word line or a selected bit line) are "half-selected". In theory, a single magnetic field should not flip the magnetisation orientation of an **SDT junction** . In practice, however, the magnetisation orientation can be flipped by a single magnetic field. If the magnetisation orientation of a half-selected **SDT junction** is flipped, an undesirable erasure occurs and an increased burden on error code correction can...

...field to the memory element.

The preferred embodiments can improve the reliability of writing to **SDT junctions** , in particular the reliability of writing to magnetic memory elements of **MRAM** devices.

Embodiments of the present invention are described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is an illustration of an **SDT junction** ;

Figures 2a and 2b are illustrations of hysteresis loops for the **SDT junction** ;

Figure 3 is an illustration of an **MRAM** device that can perform thermally-assisted switching;

Figure 4 is an illustration of a heating line for the **MRAM** device;

Figures 5a, 5b, 5c and 5d are illustrations of different patterns of heating lines for the **MRAM** device; and

Figure 6 is an illustration of a multi-level **MRAM** chip.

As shown in the drawings, the described embodiment relates to a **MRAM** device including an array of magnetic memory elements. During data storage, the **MRAM** device performs thermally-assisted switching of selected memory elements. The thermally-assisted switching improves the reliability of storing data in the **MRAM** device.

A magnetic memory element of the **MRAM** device could be any element having a resistance that is dependent upon the state of its magnetic film. Examples of such elements include magnetic tunnel **junctions** (the **SDT junction** is a type of magnetic tunnel junction) and giant magnetoresistance ("GMR") spin valves. For the purposes of illustration, the memory elements are described herein as **SDT junctions** .

Reference is made to Figure 1, which shows an **SDT junction** 10. The **SDT junction** 10 includes a pinned layer 12 having a magnetisation that is oriented in the plane...

...rotate in the presence of an applied magnetic field in a range of interest. The **SDT junction** 10 also includes a "free" layer 14 having a magnetisation orientation that is not pinned...

...12 and 14. This tunnelling phenomenon is electron spin dependent, making the resistance of the **SDT junction** 10 a function of the relative orientations of the magnetisation of the pinned and free layers 12 and 14. For instance, resistance of the **SDT junction** 10 is a first value (R) if the magnetisation orientation of the pinned and freeMagnetic fields (Hx, Hy) may be applied to the **SDT junction** 10 by supplying currents (Iy, Ix) to first and second conductors 18 and 20 contacting the **SDT junction** 10. If the conductors 18 and 20 are orthogonal, the applied magnetic fields (Hx, Hy...

...the magnitude of one or both write currents (Ix, Iy) may be reduced if the **SDT junction** 10 is heated. Coercivity of a magnetic film decreases with increasing temperature. Raising the temperature of the **SDT junction** 10 reduces the coercivity (Hc) of the **SDT junction** 10, as shown in Figures 2a and 2b. Figure 2a shows the coercivity (Hc) at ...

...the coercivity (Hc) at 50(degree)C above room temperature. At the elevated temperature, the **SDT junction** 10 switches from a high resistance state to a low resistance state and vice-versa in the presence of a lower combined magnetic field (Hx+Hy). Therefore, heating the **SDT junction** 10 allows the magnitudes of one or both of the write currents (Ix, Iy) to...

...the other hand, the magnitudes of the write currents (Ix, Iy) are not reduced, the **SDT junction** 10 will switch more reliably in the presence of the combined magnetic field (Hx+Hy...

...creates an additional magnetic field, the third conductor 22 is far enough away from the **SDT junction** 10 so that the additional magnetic field does not adversely affect the switching.

Although Figure 1 shows the third conductor 22 being above the **SDT junction** 10, the third conductor 22 may instead be below the **SDT junction** 10. Third conductors 22 may even be above and below the **SDT junction** 10.

Reference is now made to Figure 3, which illustrates an information storage device 110...

?

Thermally-assisted switching of magn tic memory elem nts

Patent Number: US2002089874
Publication date: 2002-07-11
Inventor(s): TRAN LUNG T (US); NICKEL JANICE H
Applicant(s):
Requested Patent: EP1225592
Application US20010758757 20010111
Priority Number(s): US20010758757 20010111
IPC Classification: G11C11/15
EC Classification: G11C11/16
Equivalents: CN1365117

Abstract

A magnetic memory element is written to by heating the memory element and applying at least one magnetic field to the memory element

File : INPADOC

SS Results

1	0	/CT EP1207538
2	0	/CT EP1132920
3	0	/ CT EP1225592

Search statement 4

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Set      Items   Description
S1       13748   MRAM OR MAGNETIC?()RANDOM()ACCESS()MEMOR? OR (NONVOLATILE -
             OR NON(W)VOLATILE)(W)MEMORY OR NON()VOLATILE()RAM OR NVRAM OR
             MAGNET?(3N)MEMOR?
S2        9848   (MEMORY OR STORAG? OR REGISTER OR MAGNETORESIST?)(2N)CELL?
S3          17   (SDT OR SPIN()DEPEND?()TUNNEL?)(2N)JUNCTION?
S4        2464   TMR OR TUNNEL?()MAGNETORESIS?
S5           0   (BOTTOM? OR TOP OR PRIMARY? LOWER? OR UPPER? OR SECOND??? -
             PINNED OR SENSE OR FIRST? OR INITIAL? OR ORIGINAL? OR 2ND)()F-
             ERROMAGNETIC?()LAYER?
S6           0   S1(S)S2(S)S3(S)S4
S7           0   S1(S)S2(S)S3
S8         357   S1(S)S2
S9           0   S8 AND S3
S10        213   S1(5N)S2
S11        186   S1(2N)S2
S12        176   S1(N)S2
S13         58   S12 AND PD<=20000228
S14         57   RD (unique items)
S15        123   FERROMAGNET?()LAYER?
S16          0   S15 AND S14
? show files
File 610:Business Wire 1999-2002/Oct 22
         (c) 2002 Business Wire.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File  16:Gale Group PROMT(R) 1990-2002/Oct 22
         (c) 2002 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2002/Oct 22
         (c)2002 The Gale Group
File 484:Periodical Abs Plustext 1986-2002/Oct W2
         (c) 2002 ProQuest
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File 553:Wilson Bus. Abs. FullText 1982-2002/May
         (c) 2002 The HW Wilson Co
File  95:TEME-Technology & Management 1989-2002/Oct W2
         (c) 2002 FIZ TECHNIK
File 369:New Scientist 1994-2002/Sep W4
         (c) 2002 Reed Business Information Ltd.
File 624:McGraw-Hill Publications 1985-2002/Oct 21
         (c) 2002 McGraw-Hill Co. Inc
?
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14/5,K/29 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

01463752 20001106435
Electrical characteristics of magnetic memory cells **comprising** magnetic **tunnel junctions and GaAs diodes**
Boeve, H; Sousa, RC; Freitas, PP; Boeck, Jde; Borghs, G
IMEC, Leuven, B
Electronics Letters, v36, n21, pp1782-1783, **2000**
Document type: journal article Language: English
Record type: Abstract
ISSN: 0013-5194

ABSTRACT:
Magnetic tunnel junctions have been the subject of study for use in nonvolatile magnetic memories. To cancel leakage paths in the memory array, a semiconductor switch is integrated per cell. Successful integration with GaAs diodes, dominating the cell performance, is described. Good resistance matching between both elements is essential to optimise the output characteristics. i.e. the absolute voltage or current difference between the two magnetic states.

DESCRIPTORS: GALLIUM ARSENIDE; 3 5 COMPOUNDS; MAGNETIC MEMORIES; MAGNETORESISTORS; DIRECT ACCESS MEMORIES; SEMICONDUCTOR DIODES; SEMICONDUCTOR SWITCHES; ELECTRICAL CHARACTERISTICS; CREEPING PATH
IDENTIFIERS: MAGNETISCHER TUNNELUEBERGANG; AUSGANGSKENNLINIE; Galliumarsenid; Drei-Fuenf-Verbindung

Electrical characteristics of magnetic memory cells **comprising** magnetic **tunnel junctions and GaAs diodes**
2000

14/5,K/36 (Item 8 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

01054986 I96118339310
Micromagnetic study on dynamic properties of write operation in magnetic random access memory cell
(Mikromagnetische Untersuchung der dynamischen Eigenschaften der Schreiboperation in magnetischen RAM-Zellen)
Asada, H; Matsuyama, K; Taniguchi, K
Dept. of Electr. Eng., Kyushu Univ., Fukuoka, Japan
1996 IEEE International Magnetics Conference (INTERMAG '96), 9-12 April 1996, Seattle, WA, USAIEEE Transactions on Magnetics, v32, n5, PT.1, pp4001-4003, **1996**
Document type: journal article Language: English
Record type: Abstract
ISSN: 0018-9464

ABSTRACT:
In a magnetic random access memory using a static differential signal due to the giant magnetoresistance effect, the write operation is performed by the switching of the magnetization direction in the free magnetic layer. The dynamic properties of the write operation in a sub-micron memory cell has been studied by a micromagnetic computation, which is important in order to estimate the power consumption and the access time in the memory. The magnetization switching process performed by step pulse currents have been investigated and the minimum pulse width required for the switching has been clarified. Both the minimum pulse width and the power consumption decreased with an increasing write current amplitude through the selective write operation range. The bit state switching was found to be caused by the incoherent rotation of the magnetization in the fine thin film pattern due to the demagnetization field. The dependence of the switching process on the damping constant is also discussed

DESCRIPTORS: DEGAUSSING; **MAGNETIC** FILM STORES; **MEMORY CELL** ;

MAGNETISATION ; WRITING--ACTION; DIRECT ACCESS MEMORIES; DATA STORAGE; ACCESS TIME; DIRECT ACCESS; MAGNETORESISTANCE; DISSIPATION POWER; DIRECTION OF MAGNETIZATION; IMPULSE DURATION; DAMPING CONSTANT; CONFERENCE PROCEEDINGS; MAGNETIC SWITCHING; INPUT--POWER; DYNAMIC PROPERTIES
IDENTIFIERS: GIANT MAGNETORESISTANCE; WRITE OPERATION; **MAGNETIC RANDOM ACCESS MEMORY CELL** ; STATIC DIFFERENTIAL SIGNAL; GIANT MAGNETORESISTANCE EFFECT; MAGNETIZATION DIRECTION; FREE **MAGNETIC** LAYER; SUB MICRON **MEMORY CELL** ; MICROMAGNETIC COMPUTATION; **MAGNETIZATION** SWITCHING PROCESS; MINIMUM PULSE WIDTH; WRITE CURRENT AMPLITUDE; SELECTIVE WRITE OPERATION; BIT STATE SWITCHING; INCOHERENT ROTATION; DEMAGNETIZATION FIELD; Magnetschichtspeicher; Schreiboperation
Micromagnetic study on dynamic properties of write operation in magnetic random access memory cell
1996
DESCRIPTORS: DEGAUSSING; **MAGNETIC** FILM STORES; **MEMORY CELL** ; **MAGNETISATION** ; WRITING...
IDENTIFIERS: GIANT MAGNETORESISTANCE; WRITE OPERATION; **MAGNETIC RANDOM ACCESS MEMORY CELL** ; STATIC DIFFERENTIAL SIGNAL; GIANT MAGNETORESISTANCE EFFECT; MAGNETIZATION DIRECTION; FREE **MAGNETIC** LAYER; SUB MICRON **MEMORY CELL** ; MICROMAGNETIC COMPUTATION; **MAGNETIZATION** SWITCHING PROCESS; MINIMUM PULSE WIDTH; WRITE CURRENT AMPLITUDE; SELECTIVE WRITE OPERATION; BIT STATE SWITCHING; INCOHERENT...

14/5,K/43 (Item 15 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

01014104 E96061392252
Micromagnetic study on write operation in submicron magnetic random access memory cell
(Mikromagnetische Untersuchung des Schreibvorganges in einer magnetischen Submikrometer-RAM-Zelle)
Asada, H; Matsuyama, K; Taniguchi, K
Kyushu Univ., Fukuoka, J
Journal of Applied Physics, v79, n8 Part 2B, pp6646-6648, **1996**
Document type: journal article Language: English
Record type: Abstract
ISSN: 0021-8979

ABSTRACT:
In a spin-valve random access memory, the binary bit states of the storage cell are determined by the magnetization direction in the free magnetic layer. The write operation of a submicron memory cell element has been studied by a micromagnetic computation based on an energy minimization scheme, which aids in the chip design. The magnetization of the binary states in the element was found to take a single domain structure having the opposite direction of the long-axis component. The mean long-axis component of magnetization of each binary state was +/- 0.97 without external fields. The selective switching of the bit state in the element was performed by the write currents applied into the two level conductors overlying the element for various conditions. The influence of the write currents to the neighboring element on a two-dimensional memory array with a 1 micron x 1 micron pitch was also simulated, in order to confirm the selective switching of the memory element. It was found that the selective write current amplitude decreased with an increasing assist current amplitude and the range was extended by the large difference of the transverse magnetic field between the selected and neighboring element. The effect of the exchange interaction from the pinned magnetic layer on the write operation was also discussed. (Proc. of the 40th Annual Conf. on Magnetism and Magnetic Materials)

DESCRIPTORS: **MAGNETIC MEMORIES** ; **MEMORY CELL** ; DIRECT ACCESS MEMORIES ; MAGNETISATION; WRITING--ACTION; AMPERAGE; MAGNETIC FIELD; STRIP LINES; SUBMICROMETER
IDENTIFIERS: magnetische Speicherzelle; RAM; Magnetisierung; Schreibstrom

Micromagnetic study on write operation in submicron magnetic random access memory cell

1996
DESCRIPTORS: **MAGNETIC MEMORIES** ; **MEMORY CELL** ; DIRECT ACCESS MEMORIES ; MAGNETISATION; WRITING...

14/5,K/57 (Item 29 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00540301 I91117635928
Magnetoresistive memories-analogies with ferroelectrics
(Magnetoresistive Speicher, Analogien zu Ferroelektrika)
Daughton, JM
Honeywell Inc., Solid State Electron. Center, Plymouth, MN, USA
Second Symposium on Integrated Ferroelectrics, 6-8 March 1990, Monterey, CA, USAFerroelectrics, v116, n1-2, pp175-194, **1991**
Document type: journal article Language: English
Record type: Abstract
ISSN: 0015-0193

ABSTRACT:
Both Honeywell's Magnetoresistive Random Access Memory (MRAM) technology and its antecedent, a magnetoresistive memory invested by Len Schwee, are fortunate to use common magnetic materials which are relatively stable and easy to fabricate. Magnetoresistive material properties, the MRAM cell operation (bit selection, writing and reading), general circuit strategies, and packaging are described. Analogies and comparisons with ferroelectric memory material and cell operation are discussed. Both ferroelectric memory and MRAM can fill important (and different) product niches, but both require material developments in order for them to achieve general-purpose usage: the ferroelectric material must overcome fatigue and the MRAM must overcome a small signal level. Other less significant materials developments are also needed. Once the proper material is available, a surprisingly long development cycle is needed to get products through design, process start-up, reliability tests, and (for rad hard products) radiation tests. MRAM current status and plans are briefly described. The future potential for MRAMs using 0.5 mm lithography and improved magnetoresistive materials is described

DESCRIPTORS: STATE OF THE ART; DIRECT ACCESS MEMORIES; MAGNETIC MATERIALS; READING; MAGNETORESISTANCE; FATIGUE; FERROELECTRIC MEMORY
IDENTIFIERS: FERROELECTRIC STORAGE; MAGNETORESISTIVE RANDOM ACCESS **MEMORY** ; **MRAM CELL** OPERATION; BIT SELECTION; WRITING; CIRCUIT STRATEGIES; SMALL SIGNAL LEVEL; RADIATION TESTS; PACKAGING; magnetoresistiver Speicher; Ferroelektrikum

1991
IDENTIFIERS: FERROELECTRIC STORAGE; MAGNETORESISTIVE RANDOM ACCESS **MEMORY** ; **MRAM CELL** OPERATION; BIT SELECTION; WRITING; CIRCUIT STRATEGIES; SMALL SIGNAL LEVEL; RADIATION TESTS; PACKAGING; magnetoresistiver Speicher; Ferroelektrikum
?

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Set      Items   Description
S1       18039   MRAM OR MAGNETIC?()RANDOM()ACCESS()MEMOR? OR (NONVOLATILE -
             OR NON(W)VOLATILE)(W)MEMORY OR NON()VOLATILE()RAM OR NVRAM OR
             MAGNET?(3N)MEMOR?
S2       14180   (MEMORY OR STORAG? OR REGISTER OR MAGNETORESIST?)(2N)CELL?
S3          16   (SDT OR SPIN()DEPEND?()TUNNEL?)(2N)JUNCTION?
S4        1233   TMR OR TUNNEL?()MAGNETORESIS?
S5         117   (BOTTOM? OR TOP OR PRIMARY? LOWER? OR UPPER? OR SECOND??? -
             PINNED OR SENSE OR FIRST? OR INITIAL? OR ORIGINAL? OR 2ND)()F-
             ERROMAGNETIC?()LAYER?
S6           0   S1(S)S2(S)S3(S)S4(S)S5
S7           2   S1(S)S2(S)S3(S)S5
S8          13   S1(S)S2(S)(S3 OR S5)
S9          13   S7 OR S8
?show files
File 349:PCT FULLTEXT 1979-2002/UB=20021017,UT=20021003
         (c) 2002 WIPO/Univentio
File 348:EUROPEAN PATENTS 1978-2002/Oct W02
         (c) 2002 European Patent Office
?
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9/TI,PN,PD,AN,AD,AB,K/1 (Item 1 from file: 349)

SELF-ALIGNED MRAM CONTACT AND METHOD OF FABRICATION
CONTACT DE MEMOIRE MRAM AUTO-ALIGNE ET PROCEDE DE FABRICATION
Patent and Priority Information (Country, Number, Date):
Patent: WO 200275808 A2 20020926 (WO 0275808)
Application: WO 2002US7285 20020312 (PCT/WO US0207285)

English Abstract
A method of forming self-aligned MRAM contact is disclosed. MRAM stacks including an upper of a conductive material are formed over portions of integraed circuitry. An insulating material is formed over the substrate, including the MRAM stacks with the upper layer of conductive material. The insulating material is subsequently chemically mechanically polished or etched, stopping on the upper layer of conductive material, to expose of the conductive material which are used to self-alinged MRAM contacts.

French Abstract
L'invention concerne un procede de formation d'un contact de memoire MRAM auto-aligne. Les paquets de memoire MRAM munis d'une couche superieure de materiau conducteur sont formes sur des portions de circuits integres. Un materiau isolant est forme sur le substrat, comportant les paquets de memoire MRAM munis de la couche superieure de materiau conducteur. Le materiau isolant est ensuite poli ou grave de facon mecanico-chimique, jusqu'au niveau de la couche superieure de materiau conducteur, afin d'exposer ce materiau utilise en tant que contacts MRAM auto-alignes.

Fulltext Availability:
Claims

Claim
... with said at least one selfaligned contact.

52 A memory device comprising:
at least one **magnetic random access memory cell** , said **magnetic random access memory** ceH comprising a **first ferromagnetic layer** formed over a first conductor, a second ferromagnetic layer formed over said **first ferromagnetic layer** , a nonmagnetic layer between said first and second ferromagnetic layers, and a second conductor in...

9/TI,PN,PD,AN,AD,AB,K/2 (Item 2 from file: 349)

THIN FILMS FOR MAGNETIC DEVICES
FILMS MINCES POUR DISPOSITIFS MAGNETIQUES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200245167 A2 20020606 (WO 0245167)
Application: WO 2001US44350 20011126 (PCT/WO US0144350)

English Abstract
Methods are provided for forming uniformly thin layers in magnetic devices. Atomic layer deposition (ALD) can produce layers that are uniformly thick on an atomic scale. Magnetic tunnel junction dielectrics, for example, can be provided with perfect uniformity in thickness of 4 monolayers or less. Furthermore, conductive layers, including magnetic 12, 16 and non-magnetic layers 14, can be provided by ALD without spiking and other non-uniformity problems. The disclosed methods include forming metal oxide layers by multiple cycles of ALD and subsequently reducing the oxides to metal. The oxides tend to maintain more stable interfaces during formation.

French Abstract
L'invention concerne des procedes permettant de former des couches minces uniformes dans des dispositifs magnetiques. La technique de depot de couche atomique (ALD) permet de produire a une echelle atomique des couches d'epaisseur uniforme. On peut obtenir, par exemple, des materiaux

dielectriques a jonction magnetique a effet tunnel presentant une epaisseur parfaitement uniforme de quatre monocouches ou moins. En outre, on obtient, par depot de couche atomique, des couches conductrices comprenant des couches magnetiques 12, 16 et non magnetiques 14 sans penetration et autres problemes de non-uniformite. Les procedes decrits consistent a former des couches d'oxyde metallique au moyen de plusieurs cycles de depot de couche atomique, puis a reduire les oxydes en metal. Les oxydes ont tendance a conserver des interfaces plus stables pendant la formation.

Fulltext Availability:
Claims

Claim
1. A method of fabricating a **magnetic memory cell** , comprising:
providing a substrate on which the **magnetic memory cell** is formed;
depositing a **first ferromagnetic layer** ;
depositing a dielectric layer over the **first ferromagnetic layer** ; and
depositing a second ferromagnetic layer over the dielectric layer, wherein at lease one of...

9/TI,PN,PD,AN,AD,AB,K/3 (Item 3 from file: 349)

MAGNETIC STORAGE DEVICE
MEMOIRE MAGNETIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200026918 A1 20000511 (WO 0026918)
Application: WO 99EP8368 19991102 (PCT/WO EP9908368)

English Abstract
A magnetic storage device comprises an array of magnetic memory cells (50). Each cell (50) has in electrical series connection a magnetic tunnel junction (MTJ) (30) and a Zener diode (40). The MTJ (30) comprises in sequence a fixed ferromagnetic layer (FMF) (32), a non-magnetic spacer layer (33), a tunnel barrier layer (34), a further spacer layer (35), and a soft ferromagnetic layer (FMS) (36) that can change the orientation of its magnetic moment. The material type and thickness of each layer in the MTJ (40) is selected so that the cell (50) can be written by applying a voltage across the cell, which sets the orientation of the magnetic moments of the FMF (32) and FMS (36) relative to one another. The switching is effected by means of an induced exchange interaction between the FMS and FMF mediated by the tunnelling of spin-polarised electrons in the MTJ (30). The cell (50) therefore has low power consumption during write operations allowing for fast writing and dense integration of cells (50) in an array. The mechanism used to control the array to write and sense the information stored in the cells (50) is simplified.

French Abstract
Memoire magnetique comprenant un groupement de cellules de memoire magnetique (50). Chaque cellule (50) presente un branchement electrique en serie entre une jonction tunnel magnetique (MTJ) et une diode Zener (40). La MTJ presente en sequence une couche ferromagnetique fixe (FMF) (32), une couche d'ecartement non magnetique (33), une couche barriere tunnel (34), une autre couche d'ecartement (35) et une couche ferromagnetique molle (FMS) (36) pouvant modifier l'orientation de son moment magnetique. Le type de materiau et l'epaisseur de chaque couche de la MTJ (40) sont selectionnes de facon a pouvoir effectuer l'ecriture de la cellule (50) par application d'une tension a cette cellule, ce qui regle l'orientation des moments magnetiques de la FMF (32) et de la FMS (36) l'une par rapport a l'autre. La commutation est executee au moyen d'une interaction d'echange induite entre la FMS et la FMF dans laquelle l'effet tunnel des electrons polarises en rotation du MTJ (30) joue un role. La cellule (50) consomme, par consequent, peu de courant pendant les operations d'ecriture, ce qui permet de realiser une ecriture rapide et une integration dense des cellules (50) du groupement. De ce fait, le mecanisme servant a commander l'ecriture du groupement et a detecter

l'information memorisee dans les cellules (50) est simplifie.

Fulltext Availability:
Detailed Description

Detailed Description
... the disclosure of which is incorporated herein by reference.

With reference to Fig. 1A, the **memory cell** elements are arranged vertically between parallel electrically conductive word lines 1, 2, 3 and bit...

...a denser array than is achievable with a similar line-width process for DRAMs. The **MRAM** array shown in Fig. 1 A uses memory cells 9, shown in Fig. 1 B...

...which is formed as a series of stacked layers comprising a template layer 15, a **first ferromagnetic layer** 16, a anti-ferromagnetic layer 18 a FMF 20, a tunnelling barrier layer 22, a...

9/TI,PN,PD,AN,AD,AB,K/4 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Nonvolatile magnetic storage device
Nichtfluchtige magnetische Speicheranordnung
Dispositif de memoire magnetique non volatile
PATENT (CC, No, Kind, Date): EP 1231607 A2 020814 (Basic)
APPLICATION (CC, No, Date): EP 2002090057 020213;
PRIORITY (CC, No, Date): JP 200135860 010213

ABSTRACT EP 1231607 A2
A magnetic memory device of the present invention includes a first wiring conductor having a first ability to let a current flow therethrough, a second wiring conductor having a second ability larger than the first ability to let a current flow therethrough, a magnetic memory cell having a pinned magnetic layer coupled to the second wiring conductor, a free magnetic layer coupled to the first wiring conductor and a non-magnetic layer sandwiched between the first and second magnetic layers.The first wiring conductor is made of aluminum and the second wiring conductor is made of copper.

...SPECIFICATION thus-formed nonvolatile magnetic storage device is called a magnetic random access memory (MRAM).
Each **memory cell** in the MRAM has two ferromagnetic layers. One is a storage layer having a direction...

...connected to the corresponding word line. When information is recorded (written) in a one of **memory cells** selected as desired, the word and bit lines electrically connected to the **memory cell** are selected and predetermined write currents are caused to flow respectively through the word and...

...lines according to the values of the write currents. The direction of magnetization of the **upper ferromagnetic layer** , i.e., the storage layer, changes according to a resultant magnetic field formed by the...

9/TI,PN,PD,AN,AD,AB,K/5 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Magnetic Random Access Memory with improved breakdown voltage
Magnetischer Direktzugriffspeicher mit verbesserterDurchbruchspannung
Memoire magnetique a acces aleatoire avec une tension de claquage ameliore
PATENT (CC, No, Kind, Date): EP 1207538 A1 020522 (Basic)
APPLICATION (CC, No, Date): EP 2001309220 011031;
PRIORITY (CC, No, Date): US 715476 001118

ABSTRACT EP 1207538 A1

A magnetic tunnel junction (30) includes a tunnel barrier (40) having partially processed (e.g. underoxidized) base material. Such magnetic tunnel junctions (30) may be used in Magnetic Random Access Memory ("MRAM") devices (8). The partially processed base material substantially increases breakdown voltage of the junction.

...SPECIFICATION of a word line and a bit line.

In one type of MRAM device, each **memory cell** includes an **SDT junction** . The magnetisation of an **SDT junction** assumes one of two stable orientations at any given time. These two stable orientations, parallel...

...values of '0' and '1'. The magnetisation orientation, in turn, affects the resistance of the **SDT junction** . Resistance of the **SDT junction** is a first value (R) if the magnetisation orientation is parallel and a second value (R+(DELTA)R) if the magnetisation orientation is anti-parallel. The magnetisation orientation of a **SDT junction** and, therefore, its logic state may be read by sensing its resistance state.

The SDT...made to Figure 3, which illustrates an MRAM device 8 including an array 10 of **SDT junction memory cells** 12. The **memory cells** 12 are arranged in rows and columns, with the rows extending along an x-direction and the columns extending along a y-direction. Only a relatively small number of **memory cells** 12 is shown to simplify the description of the device 8. In practice, arrays of ...

9/TI,PN,PD,AN,AD,AB,K/6 (Item 3 from file: 348)

Method of repairing defective tunnel junctions
Reparaturverfahren von defekten Tunnelubergangsvorrichtungen
Methode de reparation de jonctions de tunnel defectueuses

PATENT (CC, No, Kind, Date): EP 1195680 A2 020410 (Basic)
APPLICATION (CC, No, Date): EP 2001308323 010928;
PRIORITY (CC, No, Date): US 675755 000930

ABSTRACT EP 1195680 A2

The nominal resistance of a defective tunnel junction (30) is increased by applying one or more voltage cycles to the defective tunnel junction (30). In an MRAM device (110), in which the tunnel junctions (30) are crossed by word and bit lines (116, 118), these lines are used to apply a voltage cycle to each junction, the maximum voltage being less than the junction breakdown voltage.

...SPECIFICATION of a word line and a bit line.

In one type of MRAM device, each **memory cell** includes an **SDT junction** . The magnetization of an **SDT junction** assumes one of two stable orientations at any given time. These two stable orientations, parallel...

...values of '0' and '1.' The magnetization orientation; in turn, affects the resistance of the **SDT junction** . Resistance of the **SDT junction** is a first value (R) if the magnetization orientation is parallel and a second value...

...value. SDT junctions having a significantly low nominal resistance will be referred to as "defective" **SDT junctions** .

An **SDT junction** having a significantly low nominal resistance is unusable in an **MRAM** device. The defective **SDT junction** can cause a bit error. In a resistive cross point array that does not use switches or diodes to isolate **memory cells** from one another, the other **SDT junctions** in the same column and row as the defective **SDT junction** will also be rendered unusable. Thus, a single defective **SDT junction** can cause a column-wide error and a row-wide error.

When data is read...

9/TI,PN,PD,AN,AD,AB,K/7 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Data storage devices
Datenspeicheranordnungen
Dispositifs de memoires de donnees
PATENT (CC, No, Kind, Date): EP 1189237 A1 020320 (Basic)
APPLICATION (CC, No, Date): EP 2001307831 010914;
PRIORITY (CC, No, Date): US 663752 000915

ABSTRACT EP 1189237 A1
A data storage device (8) includes a resistive cross point array (10) of memory cells (12) each memory cell (12) including a memory element (50) and a resistive element (56) connected in series with the memory element (50). The resistive elements (56) substantially attenuate any sneak path currents flowing through shorted memory elements during read operations. The data storage device (8) may be a Magnetic Random Access Memory ("MRAM") device.

...SPECIFICATION lines 14 or 16.
Reference is now made to Figure 8, which illustrates an alternative **memory cell** 80 for the MRAM device 8. This alternative **memory cell** is shown in conjunction with an **SDT junction** . Such a **memory cell** 80 includes a multi-layer stack of materials. The stack includes first and second seed...

9/TI,PN,PD,AN,AD,AB,K/8 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Information storage device
Datenspeicheranordnung
Dispositif de memoire de donnees
PATENT (CC, No, Kind, Date): EP 1187139 A1 020313 (Basic)
APPLICATION (CC, No, Date): EP 2001306097 010716;
PRIORITY (CC, No, Date): US 652807 000831

ABSTRACT EP 1187139 A1
A sense amplifier (24) applies an operating potential to a selected bit line and an equal potential to a subset of unselected lines during a read operation on a memory cell (12) in a resistive cross point array (10) of an information storage device (8). Before a resistance state of the selected memory cell (12) is sensed, however, an input of the sense amplifier (24) is forced to a known, consistent condition The sense amplifier input may be forced to the known, consistent condition by pulling up the input to an array voltage (Vs).

...SPECIFICATION located at a cross point of a word line and a bit line.
The MRAM **memory cells** may be based on **spin dependent tunnelling** (" **SDT** ") **junctions** . A typical **SDT junction** has a pinned ferromagnetic layer, a **sense ferromagnetic layer** and an insulating tunnel barrier sandwiched between the ferromagnetic layers. A logic value may be written to an **SDT junction** by applying a magnetic field that sets the **SDT junction** 's magnetisation orientation to either parallel (logic '0') or anti-parallel (logic '1'). Relative orientation...

...of the ferromagnetic layers determine the resistance state (R or R+(DELTA)R) of the **SDT junction** .
Polymer memory is another non-volatile thin-film memory that is being considered for data...

9/TI,PN,PD,AN,AD,AB,K/9 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Ram devices

Ramspeichernanordnungen
Dispositifs de memoires RAM
PATENT (CC, No, Kind, Date): EP 1152430 A2 011107 (Basic)
EP 1152430 A3 020828
APPLICATION (CC, No, Date): EP 2001303785 010426;
PRIORITY (CC, No, Date): US 564713 000503

ABSTRACT EP 1152430 A2
A write circuit (24) for a large array (10) of memory cells (12) of a Magnetic Random Access Memory ("MRAM") device (8) comprises a column driven (32) for each memory cell block, the column drivers (32) writing to different blocks at different times. The write circuit (24) provides a controllable, bi-directional write current to selected word and bit lines (14 and 16) without exceeding breakdown limits of the memory cells (12). Additionally, the write circuit (24) spreads out the write currents over time to reduce peak currents.

...SPECIFICATION device is not limited to the specific embodiments described and illustrated above. For instance, the **memory cells** are not limited to **SDT junction** devices. Other types of devices that could be used include, but are not limited to...

9/TI,PN,PD,AN,AD,AB,K/10 (Item 7 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

MRAM device
MRAM Anordnung
Dispositif MRAM
PATENT (CC, No, Kind, Date): EP 1132920 A2 010912 (Basic)
EP 1132920 A3 020821
APPLICATION (CC, No, Date): EP 2001301769 010227;
PRIORITY (CC, No, Date): US 514934 000228

ABSTRACT EP 1132920 A2
A **spin dependent tunneling** (" **SDT** ") **junction** (30) of a **memory cell** for a **Magnetic Random Access Memory** (" **MRAM** ") device (8) includes a pinned ferromagnetic layer (38), followed by an insulating tunnel barrier (40) and a **sense ferromagnetic layer** (46). During fabrication of the **MRAM** device (8), after formation of the pinned layer (38) but before formation of the insulating tunnel barrier (40), an exposed surface of the pinned layer (38) is flattened. The exposed surface of the pinned layer (38) may be flattened by an ion etching process (110).

...ABSTRACT A2
A **spin dependent tunneling** (" **SDT** ") **junction** (30) of a **memory cell** for a **Magnetic Random Access Memory** (" **MRAM** ") device (8) includes a pinned ferromagnetic layer (38), followed by an insulating tunnel barrier (40) and a **sense ferromagnetic layer** (46). During fabrication of the **MRAM** device (8), after formation of the pinned layer (38) but before formation of the insulating...

...SPECIFICATION for data storage. More specifically, the present invention relates to a method of fabricating a **magnetic random access memory** device including an array of **spin dependent tunneling junction memory cells** .
Magnetic Random Access Memory ("MRAM") is a non-volatile memory that is being considered for...

...of external power. Therefore, ideal memory cells are non-volatile.
In practice, however, not all **memory cells** are ideal. In an MRAM memory device including thousands and thousands of **SDT junction memory cells** , certain **SDT junctions** will exhibit low resistance in a zero magnetic field. When a sufficient magnetic field is...

...will inadvertently switch back to the low resistance when the magnetic

field is removed. Such **SDT junctions** are unusable.
Certain SDT junctions will switch from one magnetization orientation to the other in...

...the first and second ferromagnetic layers.
This method may be applied to MRAM devices including **SDT junction memory cells** . Steps for fabricating such **MRAM** devices include depositing a **first ferromagnetic layer** ; and flattening an exposed surface of the first layer. The exposed surface is flattened prior to depositing other layers atop the **first ferromagnetic layer** .
Other aspects and advantages of the present invention will become apparent from the following detailed...

...MRAM device according to the present invention;
Figure 2 is an illustration of an MRAM **memory cell** including an **SDT junction** , the **SDT junction** having and top and **bottom ferromagnetic layers** ;
Figures 3a and 3b are illustrations of parallel and anti-parallel magnetization orientations in the...

...present invention is embodied in an MRAM device. The MRAM device includes an array of **SDT junction memory cells** whose **bottom ferromagnetic layers** are ion etched. Ion etching the **bottom ferromagnetic layers** can increase the usable number of **SDT junctions** in the **MRAM** device. The ion etching can reduce ferromagnetic coupling in the **SDT junctions** , which can reduce the number of **SDT junctions** having high resistance in ...also tune the ferromagnetic coupling to improve symmetry of the electrical response loops of the **SDT junctions** , and it can reduce the number of shorted **SDT junctions** .
Ion etching the bottom ferromagnetic layers allows tunnel barrier thickness to be reduced. Reducing the...

...made to Figure 1, which illustrates an MRAM device 8 including an array 10 of **SDT junction memory cells** 12. The **memory cells** 12 are arranged in rows and columns, with the rows extending along an x-direction and the columns extending along a y-direction. Only a relatively small number of **memory cells** 12 are shown to simplify the description of the invention. In practice, arrays of any...

...CLAIMS A2
1. An **SDT junction** (30) of a **memory cell** for an **MRAM** device (8), the junction (30) comprising:
a bottom ferromagnetic layer (38), the bottom ferromagnetic layer...

...the AF coupling to a desired level.
6. An MRAM device comprising an array of **memory cells** with **SDT junctions** according to any preceding claim.
7. A method of fabricating a memory device including a...

9/TI,PN,PD,AN,AD,AB,K/11 (Item 8 from file: 348)

Magnetoresistive memory devices
Magnetoresistiven Speicheranordnungen
Dispositifs de memoire magnetoresistives
PATENT (CC, No, Kind, Date): EP 936624 A2 990818 (Basic)
EP 936624 A3 000920
APPLICATION (CC, No, Date): EP 99300848 990204;
PRIORITY (CC, No, Date): US 21352 980210

ABSTRACT EP 936624 A2
Magnetoresistive devices are disclosed which include a changeable magnetic region within which at least two magnetic states can be imposed. Upon magnetoresistive electrical interaction with the device, the relative orientation of the magnetic states of the changeable magnetic region, and a proximate reference magnetic region, can be sensed thereby providing a binary data storage capability. The present invention limits the electrical interaction to only a preferred portion of the changeable

magnetic region, e.g., the portion within which the two magnetic states can be dependably predicted to be substantially uniform, and opposite of one another. Structures for limiting the electrical interaction to this preferred portion of the changeable magnetic region are disclosed, and include smaller interaction regions, and alternating areas of insulation and conductive, interaction regions, disposed proximate the changeable magnetic region. The principles of the present invention can be applied to magnetic random access memory ("MRAM") arrays, which employ giant magnetoresistive ("GMR") cells, or magnetic tunnel junction ("MTJ") cells, at the intersections of bitlines and wordlines, and also to magnetic sensors such as magnetic data storage devices having access elements used to access data on a magnetic data storage medium.

...SPECIFICATION is designed so that the write currents do not pass through the MTJ itself. The **memory cell** is read by passing a sense current perpendicularly through the diode and MTJ from the...

...the junction are those which traverse perpendicular to the junction layer. The state of the **memory cell** is determined by measuring the resistance of the **memory cell** when a sense current, much smaller than the write currents, is passed perpendicularly through the...

...sense or read current is negligible and does not affect the magnetic state of the **memory cell** . The probability of tunneling of charge carriers across the tunnel barrier depends on the relative...
...the ferromagnetic layer at the interface of the ferromagnetic layer with the tunnel barrier. The **first ferromagnetic layer** tunnel barrier thus acts as a spin filter. The probability of tunneling of the charge...

...magnetic moment of the second ferromagnetic layer is aligned to the magnetic moment of the **first ferromagnetic layer** , there are more available electronic states than when the magnetic moment of the second ferromagnetic layer is aligned anti-aligned to that of the **first ferromagnetic layer** . Thus. the tunneling probability of the charge carriers is highest when the magnetic moments of...

...of the free layer uniquely define two possible bit states (0 or 1) of the **memory cell** .
In accordance with the present invention, and with reference to Fig. 7, exemplary preferred portions...

9/TI,PN,PD,AN,AD,AB,K/12 (Item 9 from file: 348)

Magnetic tunnel junction devices
Magnetische Tunnelubergangsvorrichtungen
Dispositifs a jonction tunnel magnetique
PATENT (CC, No, Kind, Date): EP 936623 A2 990818 (Basic)
EP 936623 A3 000920
APPLICATION (CC, No, Date): EP 99300847 990204;
PRIORITY (CC, No, Date): US 21515 980210

ABSTRACT EP 936623 A2
Magnetic memory cells include a changeable magnetic region with a magnetic axis along which two directions of magnetization can be imposed, thereby providing two respective states into which the cells are changeable according to electrical and resultant magnetic stimuli applied thereto. Asymmetry in the magnetic stimuli applied to the cell while writing a state therein is disclosed to provide a predictable magnetization pattern evolution from the first direction to the second direction. Physical asymmetry in the layout and/or magnetization of the cell is also disclosed which provides the predictable pattern evolution. These principles can be applied to magnetic random access memory (MRAM) arrays which employ magnetic tunnel junction (MTJ) cells at the intersections of bitlines and wordlines which supply the electrical and resultant magnetic stimuli to write the cells therein.

...SPECIFICATION is designed so that the write currents do not pass through the MTJ itself. The **memory cell** is read by passing a sense current perpendicularly through the diode and MTJ from the...

...the junction are those which traverse perpendicular to the junction layer. The state of the **memory cell** is determined by measuring the resistance of the **memory cell** when a sense current, much smaller than the write currents, is passed perpendicularly through the...

...sense or read current is negligible and does not affect the magnetic state of the **memory cell** . The probability of tunneling of charge carriers across the tunnel barrier depends on the relative...

...the ferromagnetic layer at the interface of the ferromagnetic layer with the tunnel barrier. The **first ferromagnetic layer** tunnel barrier thus acts as a spin filter. The probability of tunneling of the charge...

...magnetic moment of the second ferromagnetic layer is aligned to the magnetic moment of the **first ferromagnetic layer** , there are more available electronic states than when the magnetic moment of the second ferromagnetic layer is aligned anti-aligned to that of the **first ferromagnetic layer** . Thus, the tunneling probability of the charge carriers is highest when the magnetic moments of...

...of the free layer uniquely define two possible bit states (0 or 1) of the **memory cell** .
In accordance with the present embodiment, a form of stimulus asymmetry, i.e., "off-axis...

9/TI,PN,PD,AN,AD,AB,K/13 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Magnetic memory devices having multiple magnetic tunnel junctions therein
Magnetische Speicheranordnungen mit einer Vielzahl magnetischer Tunnelverbindungen
Dispositifs de memoires magnetique incorporant plusieurs jonctions magnetiques de tunnel

PATENT (CC, No, Kind, Date): EP 936622 A2 990818 (Basic)
EP 936622 A3 001108
EP 936622 B1 021002
APPLICATION (CC, No, Date): EP 99300384 990120;
PRIORITY (CC, No, Date): US 21342 980210

ABSTRACT EP 936622 A2
Magnetic memory devices are disclosed having multiple magnetic tunnel junctions therein writable together into an average state. For example, a magnetic random access memory ("MRAM") array is disclosed having respective pluralities of crossing first and second electrically conductive lines forming a plurality of intersecting regions across the array. The array includes a plurality of magnetic memory cells, each disposed at a respective one of the plurality of intersecting regions. Each cell includes at least two magnetic tunnel junctions therein, writable together into an average state, according to electrical and resultant magnetic stimuli applied thereto via a respective first and second conductive line. The at least two magnetic tunnel junctions provided in each magnetic memory cell provide a predictable magnetic response for all cells across the array. Only the cell at an intersecting region selected by stimuli applied via each of the first and second electrically conductive lines forming the selected region is written, and other cells along the first and second electrically conductive lines forming the selected region are not written. An operating window of applied electrical and therefore magnetic stimuli can be defined to ensure cell selectivity across the memory array.

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In accordance with the present invention, and with reference to Fig. 9, a magnetic memory...

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